Product Features

- Compliant with IEEE Std 802.3cd
- Compliant with 400G-FR4 optical specifications
- Compliant with OSFP MSA
- Compliant with CMIS Management interface specifications
- Duplex LC receptacles
- 53.125GBd PAM4x4 un-cooled EA-DFB LD
- 26.5625GBd PAM4x8 electrical connector
- Transmission distance up to 2km
- Single +3.3V power supply
- Commercial operating temperature:0°C to +70°C
- RoHS Compliant

Applications

- 400G BASE-FR4 Ethernet
- Coarse wavelength division multiplexing systems

Descriptions

LX9104CDR transceiver is designed for use in 400Gb/s network applications, the maximum transmission distance is 2km. LX9104CDR is a fully integrated optical transceiver modulated using 4-level pulse amplitude modulation (PAM4) format that transmits and receives optical signals with aggregated data rate of 425Gbps over 4 lanes on CWDM wavelength grids each running at 106.25Gbps.They are compliant with the OSFP MSA and 400GBASE-FR4 optical specifications. LX9104CDR are compliant with RoHS.

Ordering Information

Table 1. Ordering Information

Part Number	Transmitter	Output Power (OMA each lane)	Receiver	Sensitivity (OMA each lane)	Reach	Temp	DDM	RoHS
LX9104CDR	CWDM EML	-0.3 ~ +3.7dBm	PIN	< -4.6dBm	2km	0~ 70 °C	Available	Compliant

Pin Description

Table 2. Pin Description

Pin	Name	Function/Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	

6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-wire Serial interface clock	LVCMOS-I/O	Bi-directional	3	1
15	VCC	+3.3V Power		Power from Host	2	
16	VCC	+3.3V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode / Module Present	Multi-Level	Bi-directional	3	2
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	2

45	VCC	+3.3V Power		Power from Host	2	
46	VCC	+3.3V Power		Power from Host	2	
47	SDA	2-wire Serial interface data	LVCMOS-I/O	Bi-directional	3	1
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Notes:

1. Open-Drain with pull-up resistor on host.
2. See pin description of OSFP MSA for required circuit.

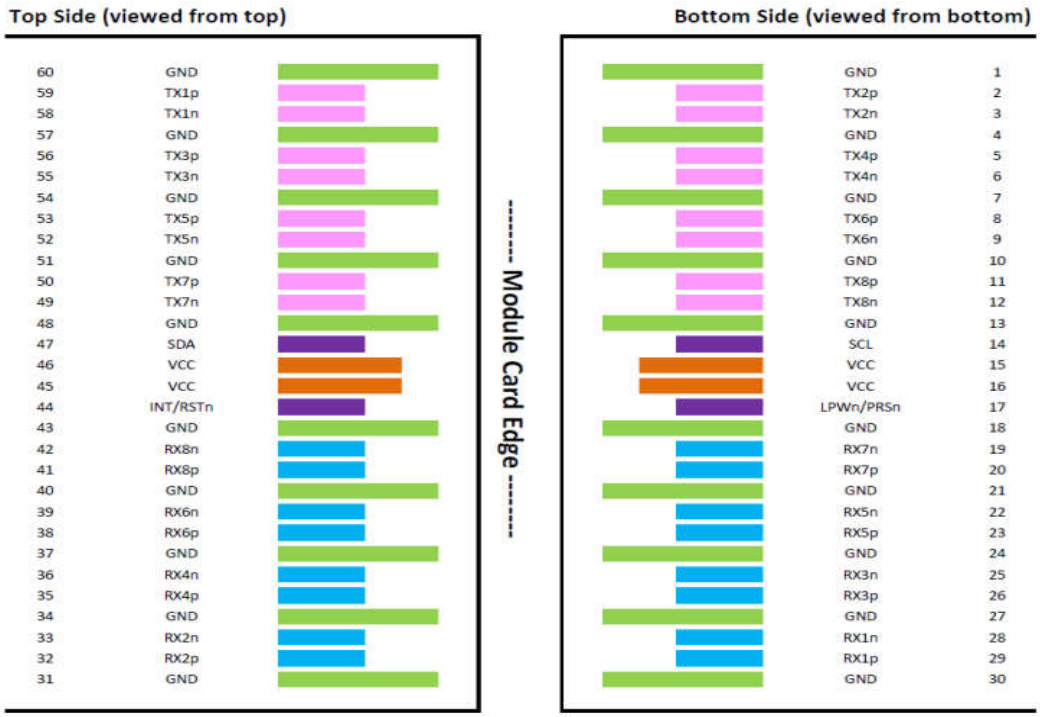


Figure 1. Host PCB OSFP pad assignment

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T_S	-40	85	°C
Relative Humidity	RH	15	85	%
Supply Voltage	V_{CC}	-0.5	4.0	V

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T_C	0	25	70	°C
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate PER Channel	-	-	53.125	-	GBd
Modulation format			PAM4		

Transceiver Electrical Characteristics

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	Icc	-	-	2.9	A	-
Power Dissipation	P_D	-	-	9	W	-
Transmitter						
Input Differential Impedance	Z_{IN}	-	100	-	Ω	-
Differential Data Input Swing	$V_{IN, P-P}$	180	-	900	mV_{P-P}	-
Receiver						
Output Differential Impedance	Z_O	-	100	-	Ω	-
Differential Data Output Swing	$V_{OUT, P-P}$	300	-	850	mV_{P-P}	1

Notes:
1. Internally AC coupled, but requires a external 100Ω differential load termination.

Transmitter Optical Characteristics

Table 6. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Lane wavelengths	λc	1264.5	-	1277.7	nm	1
		1284.5	-	1297.5		
		1304.5	-	1317.5		
		1324.5	-	1337.5		
Side-mode suppression ratio	SMSR	30	-	-	dB	-
Total average launch power	P_T	-	-	9.3	dBm	-
Average launch power, each lane	P	-3.3	-	3.5	dBm	-
Outer Optical Modulation Amplitude, each lane	OMA outer	-0.3	-	3.7	dBm	-
Difference in launch power between any two lanes(OMA outer)	-	-	-	4	dB	-
Transmitter and dispersion penalty eye closure for PAM4, each lane	TDECQ	-	-	3.4	dB	-
Extinction Ratio	EX	3.5	-	-	dB	-
Average launch power of OFF transmitter	P_{off}	-	-	-30	dBm	-
Optical Return Loss Tolerance	ORLT	-	-	17.1	dB	-
Transmitter reflectance	-	-	-	-26	dB	-

Notes:
1. The typical wavelengths compliant with 1310nm CWDM wavelength grids.

Receiver Optical Characteristics

Table 7. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Lane Wavelength	λc	1264.5	-	1277.7	nm	-
		1284.5	-	1297.5		
		1304.5	-	1317.5		
		1324.5	-	1337.5		
Average Receiver Power, each lane	P	-7.3	-	3.5	dBm	-
Receiver Overload (Average Power)	P_{OL}	3.5	-	-	dBm	-
Damage Threshold	P_{TH}	4.5	-	-	dBm	-
Receive power, each lane (OMA outer)	OMA	-	-	3.7	dBm	-
Receiver Sensitivity each lane (OMA outer)				-4.6	dBm	1
Optical Reflectance	ORL	-	-	-26	dB	-
LOS De-Assert	LOS_D	-	-	-10	dBm	-
LOS Assert	LOS_A	-16	-	-	dBm	-
LOS Hysteresis	-	0.5	-	-	dB	-

Notes:
1. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, BER<2.4E^{-4}.

Recommended Host Board Power Supply Filter Network

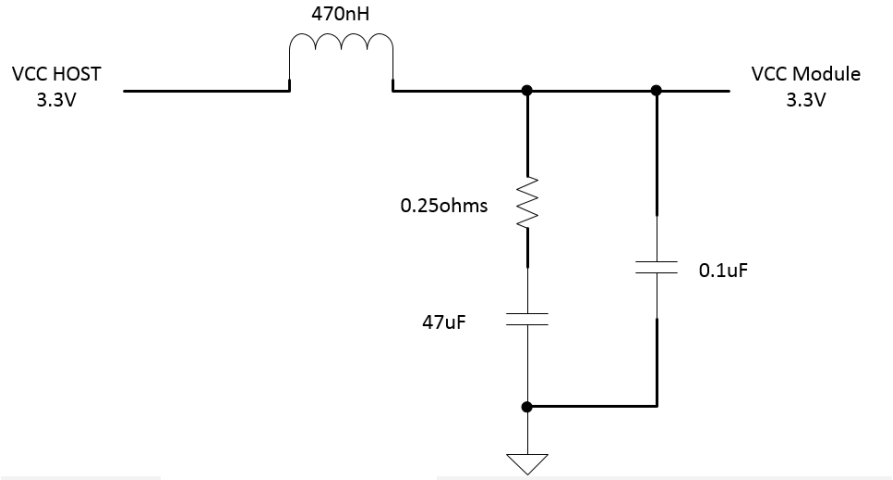


Figure 2. Recommended Host Board Power Supply Filter Network

Recommended Application Interface Block Diagram

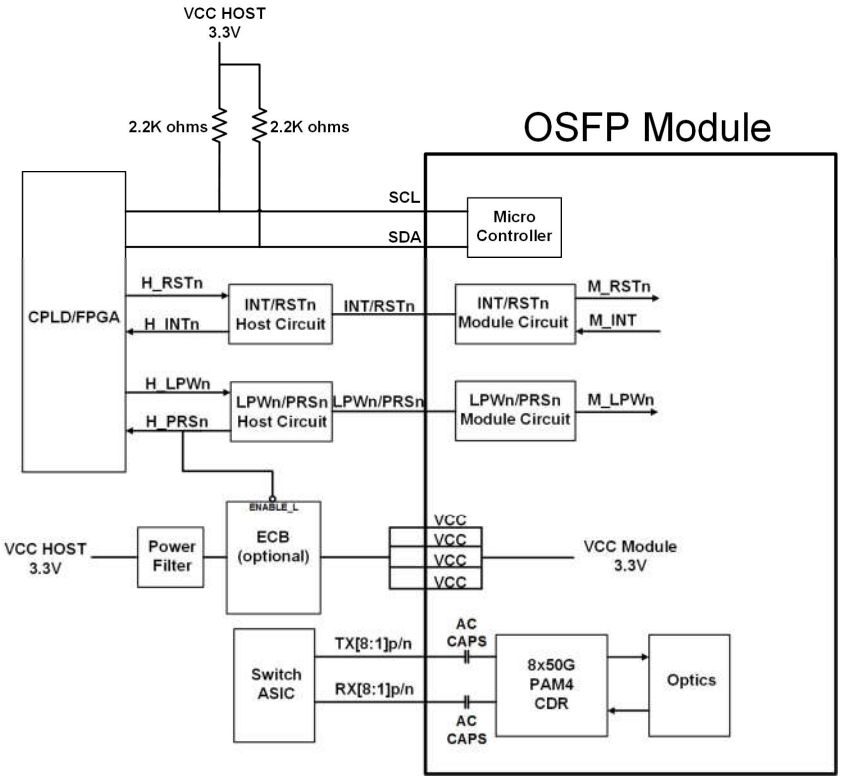


Figure 3. Recommended Application Interface Block Diagram

Mechanical specifications

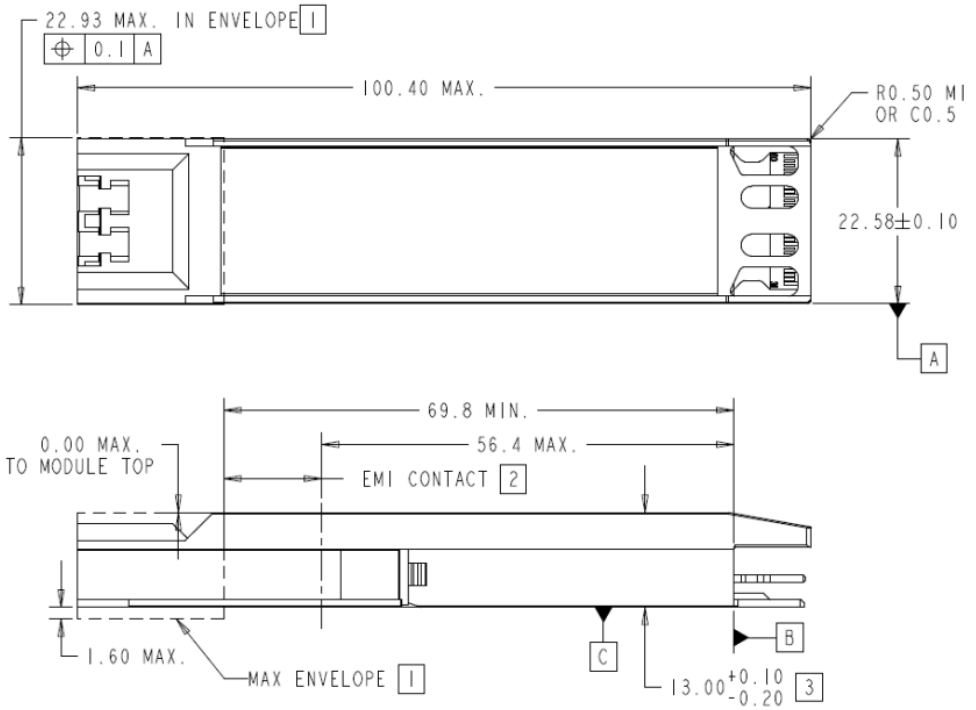
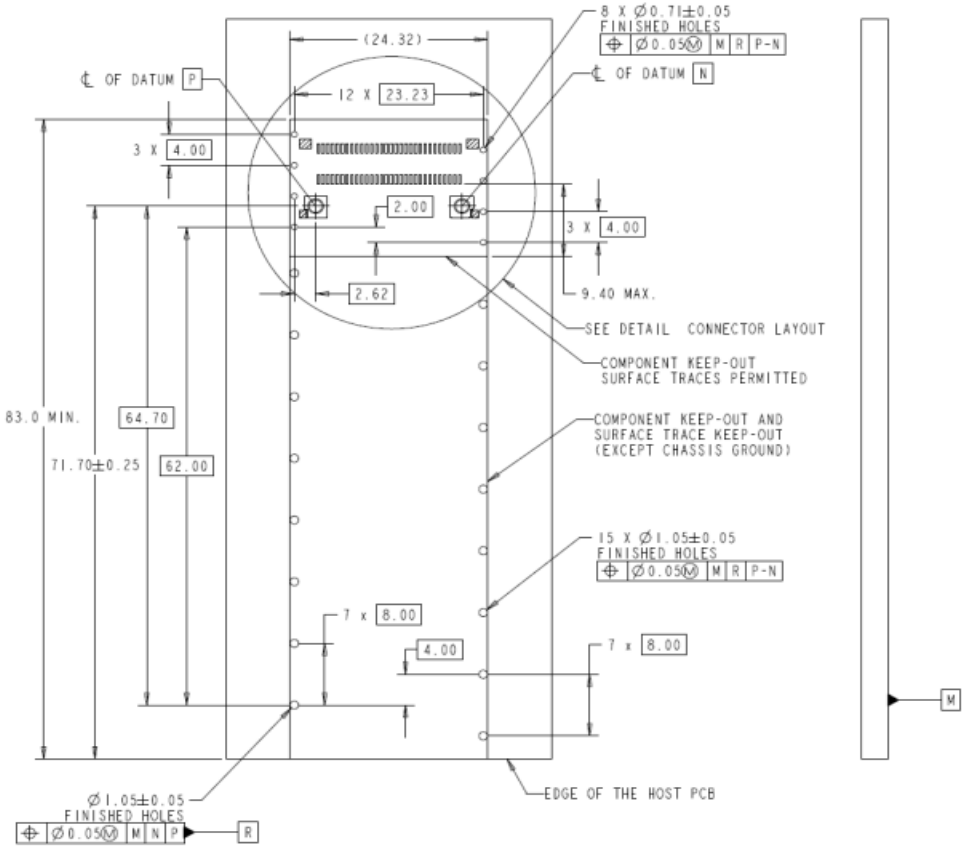


Figure 4. Outline Drawing

PCB Layout Recommendation



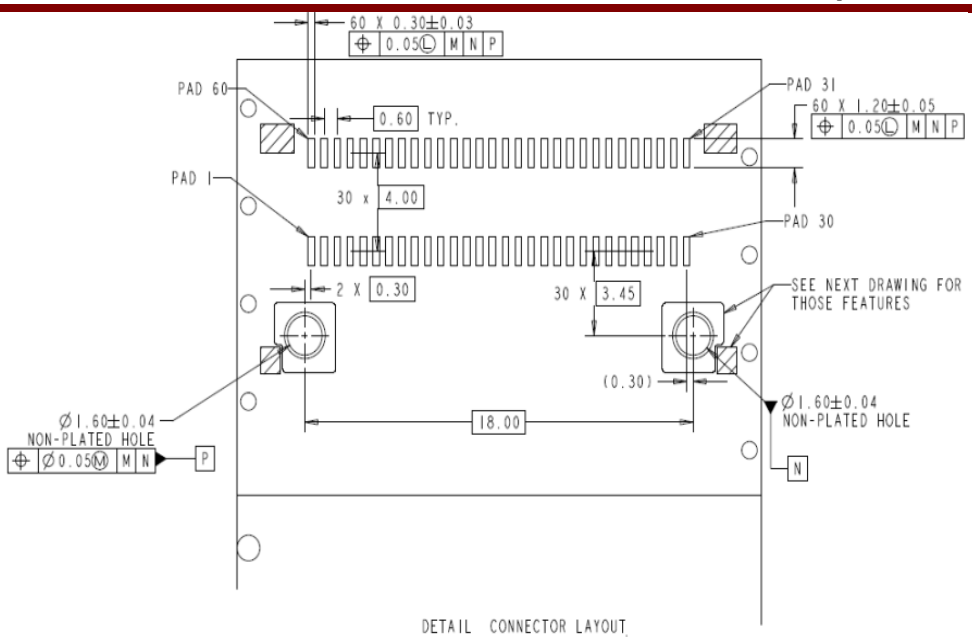


Figure 5. PCB layout recommendation

RoHS Compliance

RoHS Certificate Number: BST13080782Y-1RC-4, compliance with the council RoHS directive-2011/65/EU.

Revision History

Date	Rev	Description	Modified By
12/21/2019	V0.1	Preliminary Release	Hui Yang

For More Information

Linktel Technologies Co., Ltd

info@linkteltech.com

www.linkteltech.com

Linktel USA

1601 McCarthy Blvd #9, Milpitas, CA 95035, USA

Tel: +1 408 807 0482

Email: linktelus@linkteltech.com

jimli@linkteltech.com

Linktel International (Except USA)

E12, No. 52 Liufang Road, East-Lake Hi-tech Development Zone, Wuhan, China

Tel: +86 27 8792 9207

Email: ailsagong@linkteltech.com

Linktel China

E12, No. 52 Liufang Road, East-Lake Hi-tech Development Zone, Wuhan, China

Tel: +86 27 8792 9213

Email: lifan@linkteltech.com