

Product Features

- Compliant with IEEE Std 802.3-2005
- Electrical interface specifications per SFF-8431
- Management interface specifications per SFF-8431 and SFF-8472
- SFP+ MSA package with duplex LC connector
- Uncooled DML Laser
- Up to 10.3Gb/s bi-directional data links
- Single +3.3V power supply
- Class 1 laser safety certified
- Industrial operating temperature: -5°C to +70 °C
- Up to 10km on 9/125µm SMF
- RoHS Compliant



Applications

- 10G Ethernet 10GBASE-LR/LW
- 10km 10G CWDM Network

Descriptions

LX436xCDR-CA7 SFP+ transceivers, according to Enhanced 8.5 and 10 Gigabit Small Form Factor Pluggable “SFP+” Multi-Sourcing Agreement (MSA) SFF-8431 and SFF-8472, revision 12.2, are designed for CWDM 10G data communications up to 10km over single mode fiber. They are compliant with IEEE Std 802.3-2005 10Gb Ethernet.

LX436xCDA are compliant with RoHS.

Ordering Information

Table 1. Ordering Information

Part Number	Transmitter	Output Power	Receiver	Sensitivity	Reach	Temp	DDM	RoHS
LX4361CDR-CA7	1471nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4362CDR-CA7	1491nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4363CDR-CA7	1511nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4364CDR-CA7	1531nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4365CDR-CA7	1551nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4366CDR-CA7	1571nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4367CDR-CA7	1591nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant
LX4368CDR-CA7	1611nm DML	-3 ~ 2dBm	PIN	< -14dBm	10km	-5 ~ 70°C	Available	Compliant

Pin Description

Table 2. Pin Description

Pin	Name	Function/Description	Notes
1	VeeT	Transmitter Ground	1
2	TX_Fault	Transmitter Fault (LVTTTL-O) - High indicates a fault condition	2
3	TX_Disable	Transmitter Disable (LVTTTL-I) – High or open disables the transmitter	3
4	SDA	Two wire serial interface Data Line (LVCMOS-I/O) (MOD-DEF2)	4
5	SCL	Two wire serial interface Clock Line (LVCMOS-I/O) (MOD-DEF1)	4
6	MOD_ABS	Module Absent (Output), connected to VeeT or VeeR in the module	5
7	RS0	Rate Select 0 – Not used, Presents high input impedance	-
8	RX_LOS	Receiver Loss of Signal (LVTTTL-O)	2
9	RS1	Rate Select 1 – Not used, Presents high input impedance	-
10	VeeR	Receiver Ground	1
11	VeeR	Receiver Ground	1
12	RD-	Inverse Received Data out (CML-O)	-
13	RD+	Received Data out (CML-O)	-
14	VeeR	Receiver Ground	-
15	VccR	Receiver Power - +3.3V	-
16	VccT	Transmitter Power - +3.3 V	-
17	VeeT	Transmitter Ground	1
18	TD+	Transmitter Data In (CML-I)	-
19	TD-	Inverse Transmitter Data In (CML-I)	-
20	VeeT	Transmitter Ground	1

Notes:

1. The module signal grounds are isolated from the module case.
2. This is an open collector/drain output that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.
3. This input is internally biased high with a 4.7KΩ to 10KΩ pull-up resistor to VccT.
4. Two-Wire Serial interface clock and data lines require an external pull-up resistor dependent on the capacitance load.
5. This is a ground return that on the host board requires a 4.7KΩ to 10KΩ pull-up resistor to VccHost.

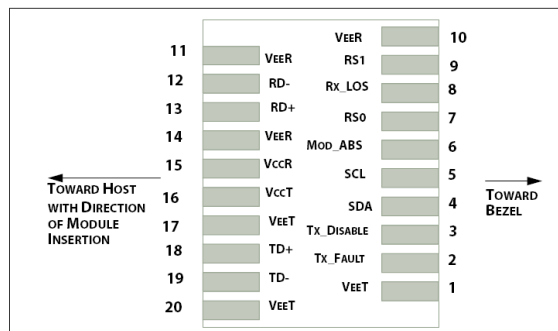


Figure 1. Host PCB SFP+ pad assignment top view

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T _s	-40	85	°C
Relative Humidity	RH	5	95	%
Supply Voltage	V _{CC}	-0.5	4.0	V

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Temperature	T _c	-5	25	70	°C
Supply Voltage	V _{CC}	3.135	3.3	3.465	V
Data Rate	-	-	10.3125	-	Gb/s

Transceiver Electrical Characteristics

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes	
Module Supply Current	I _{CC}	-	-	300	mA	-	
Power Dissipation	P _D	-	-	1000	mW	-	
Transmitter							
Input Differential Impedance	Z _{IN}	-	100	-	Ω	-	
Differential Data Input Swing	V _{IN, P-P}	190	-	700	mV _{P-P}	-	
TX_FAULT	Transmitter Fault	V _{OH}	2.0	-	V _{CCHOST}	V	-
	Normal Operation	V _{OL}	0	-	0.8	V	-
TX_DISABLE	Transmitter Disable	V _{IH}	2.0	-	V _{CCHOST}	V	-
	Transmitter Enable	V _{IL}	0	-	0.8	V	-
Receiver							
Output Differential Impedance	Z _O	-	100	-	Ω	-	
Differential Data Output Swing	V _{OUT, P-P}	300	-	850	mV _{P-P}	1	
RX_LOS	Loss of signal (LOS)	V _{OH}	2.0	-	V _{CCHOST}	V	2
	Normal Operation	V _{OL}	0	-	0.8	V	2

Notes:

- Internally AC coupled, but requires a external 100Ω differential load termination.
- LOS is an open collector output. Should be pulled up with 4.7KΩ on the host board.

Transmitter Optical Characteristics

Table 6. Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
MAX. Output Power (P_{avg})	P_{out}	-3	-	+2	dBm	1
Center Wavelength Range	λ_c	1464.5	1471	1477.5	nm	-
		1484.5	1491	1497.5	nm	-
		1504.5	1511	1517.5	nm	-
		1524.5	1531	1537.5	nm	-
		1544.5	1551	1557.5	nm	-
		1564.5	1571	1577.5	nm	-
		1584.5	1591	1597.5	nm	-
		1604.5	1611	1617.5	nm	-
Center Wavelength Tolerance	$\Delta\lambda_c$	-6.5	-	6.5	nm	-
Extinction Ratio	EX	3.5	-	-	dB	2
Optical Return Loss Tolerance	ORLT	-	-	24	dB	-
Spectral Width (-20dB)	$\Delta\lambda$	-	-	1	nm	-
Side Mode Suppression Ratio	SMSR	30	-	-	dB	-
P_{out} @TX-Disable Asserted	P_{off}	-	-	-45	dBm	1
Eye Diagram	IEEE Std 802.3-2005 10Gb Ethernet 10GBASE-LR compatible					

Notes:

1. The optical power is launched into 9/125 μ m SMF.
2. Measured with a PRBS7, 9 or 31 test pattern.

Receiver Optical Characteristics

Table 7. Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Center Wavelength	λ_c	1260	-	1620	nm	-
Receiver Sensitivity (P_{avg})	S	-	-	-14	dBm	1
Receiver Overload (P_{avg})	P_{OL}	1	-	-	dBm	1
LOS De-Assert	LOS_D	-	-	-15	dBm	-
LOS Assert	LOS_A	-3	-	-	dBm	-
LOS Hysteresis	-	0.5	-	5	dB	-

Notes:

1. Measured with a PRBS31 test pattern, 10.3Gb/s, BER<10⁻¹².

Digital Diagnostic Memory Map

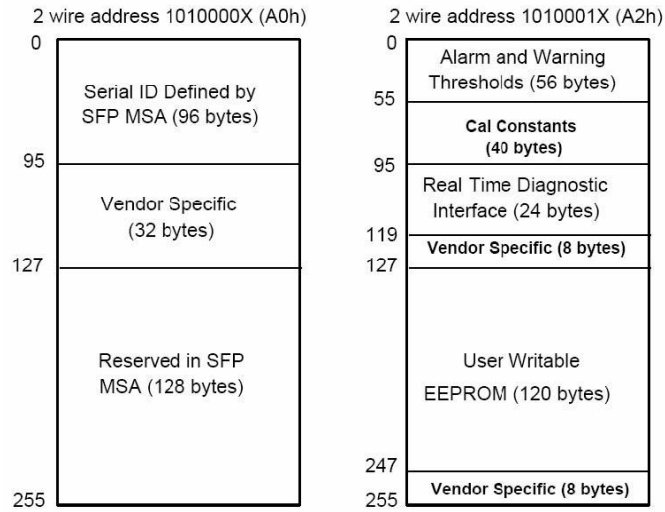


Figure 2. Digital Diagnostic Memory Map Specific Data Field Descriptions

Recommended Host Board Power Supply Filter Network

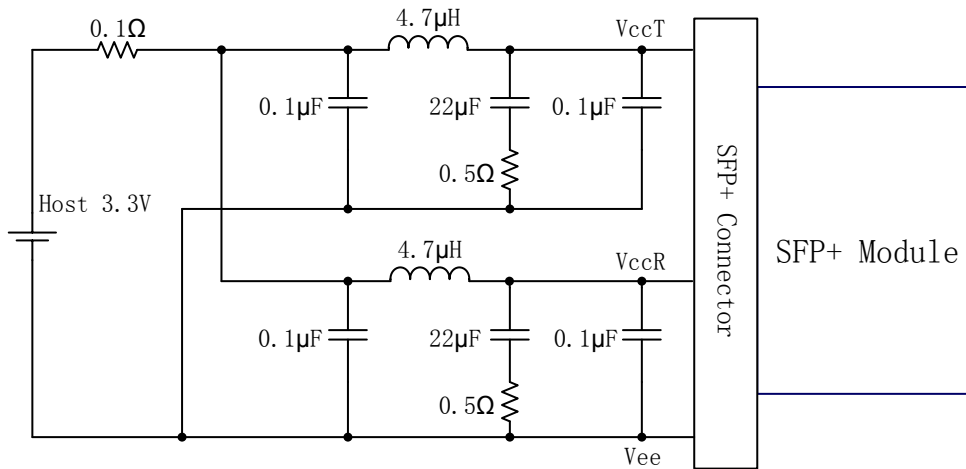


Figure 3. Recommended Host Board Power Supply Filter Network

Recommended Application Interface Block Diagram

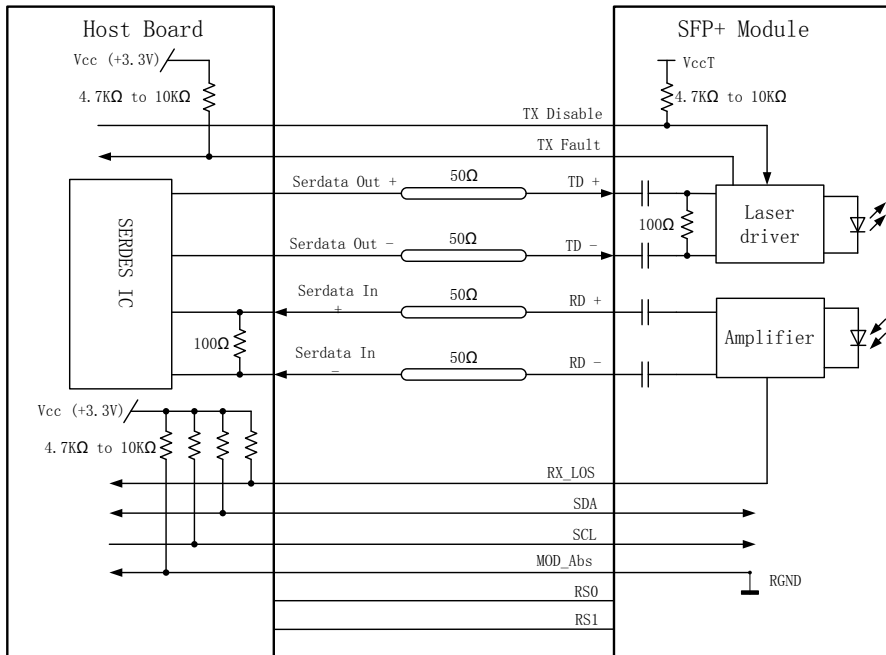


Figure 4. Recommended Application Interface Block Diagram

Mechanical specifications

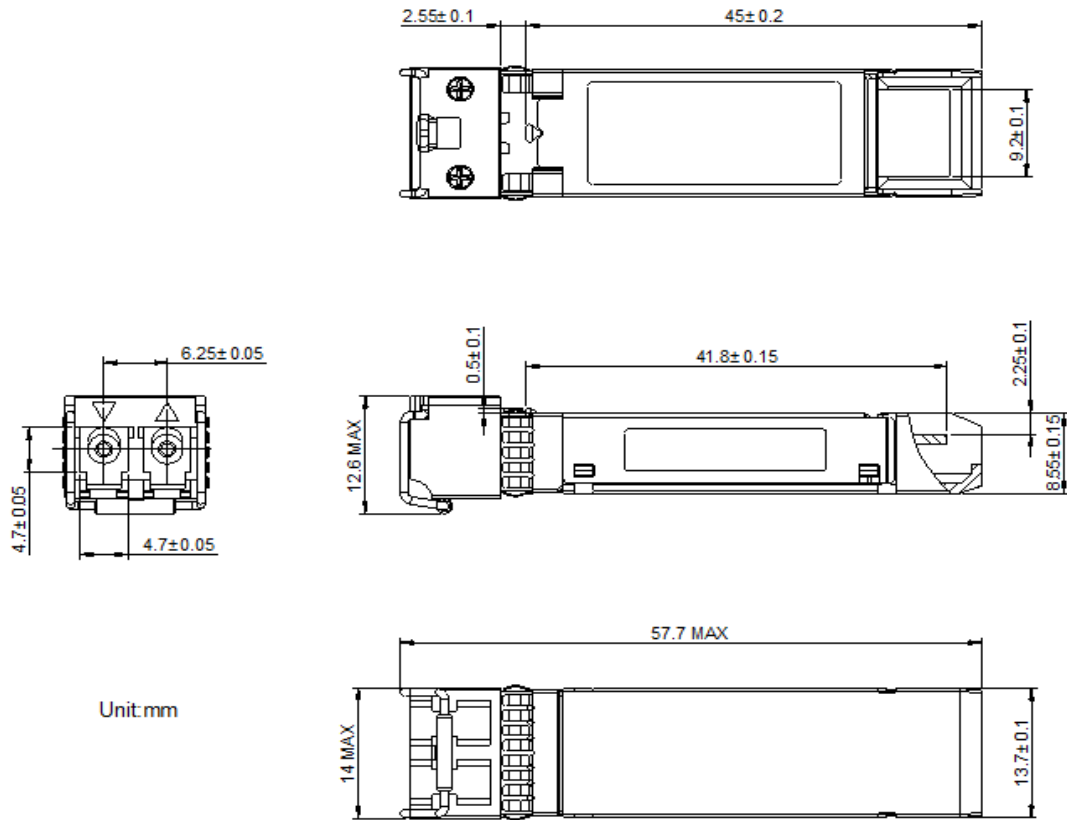


Figure 5. Outline Drawing

PCB layout recommendation

- Notes:
1. Datum and basic dimensions established by customer
 2. Pads and vias are chassis ground, 11 places
 3. Thru holes, plating optional

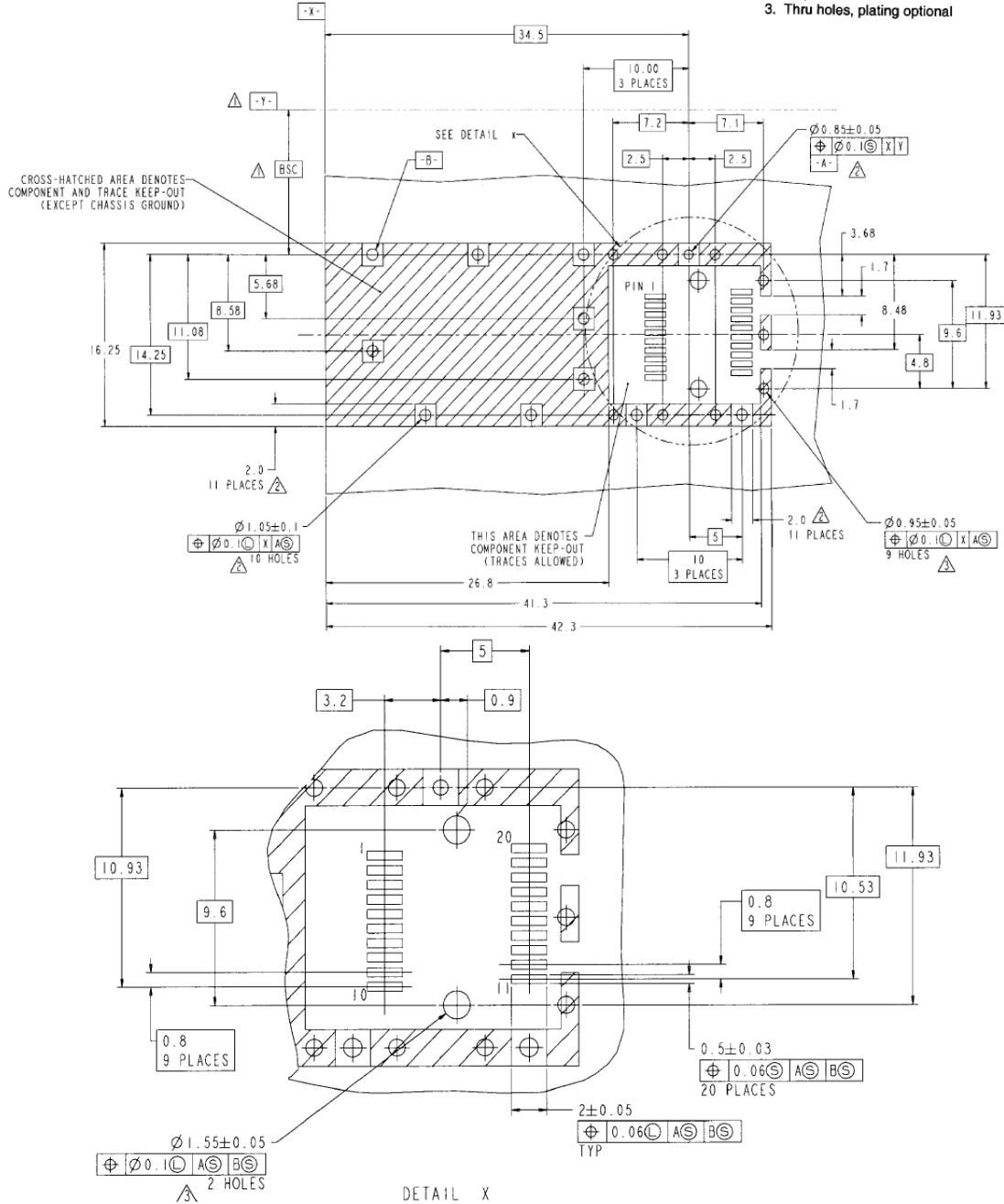


Figure 6. PCB layout recommendation

Revision History

Date	Rev	Description	Modified By
3/2/2021	VB.00	initial version	Xun Sun

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