Product Features

- Up to 1.25Gb/s bi-directional data links
- SFP form with compact RJ-45 connector
- +3.3V single power supply
- Operating case temperature
  Commercial: -10ºC to +70ºC
- Intelligent Auto-Negotiation
  support for automatic duplex, speed,and
  flow control resolution
- Only 1000Base-T with SerDes interface
- Fully metallic enclosure for low EMI
- Access to physical layer IC via 2-wire serial bus
- RoHS compliant and Lead Free

Applications

- Switch to Switch interface
- 1.25 Gigabit Ethernet over Cat 5 cable

Descriptions

1000BASE-T Copper Small Form Pluggable (SFP) transceivers are based on the SFP Multi Source Agreement (MSA). They are compatible with the Gigabit Ethernet and 1000BASE-T standards as specified in IEEE Std 802.3. The 1000BASE-T physical layer IC (PHY) can be accessed via I2C, allowing access to all PHY settings and features.

Through Copper SFP transceiver, the 1000BASE-X fiber Auto-negotiation on the host board side is transparently converted to 1000BASE-T Auto-negotiation on the copper side. The host systems used to work with fiber SFPs will also work with copper SFPs, so there is no need to change MAC software.

Ordering Information

Table 1. Ordering Information

Part Number	Package	Data rate	Interface	Auto-negotiation	LOS Pin	Temp	Reach	RoHS
LX1801CNL	SFP	1000M	SerDes	YES	YES	-10~ 70 ºC	100m	Compliant

Pin Description

Table 2. Pin Description

Pin	Name	Function/Description	Engagement order (Insertion)	Notes
1	VeeT	Transmitter Ground	1	-
2	TX Fault	Transmitter Fault Indication (not supported)	3	
3	TX Disable	Transmitter Disable	3	Note 1
4	MOD-DEF2	Module Definition 2-Two wire serial ID interface	3	Note 2
5	MOD-DEF1	Module Definition 1-Two wire serial ID interface	3	Note 2
6	MOD-DEF0	Module Definition 0-Grounded in module	3	Note 2
7	Rate Select	Not Connected	3	-
8	LOS	Loss of Signal	3	Note 3
9	VeeR	Receiver Ground	1	-
10	VeeR	Receiver Ground	1	-
11	VeeR	Receiver Ground	1	-
12	RD-	Inverse Received Data out	3	Note 4
13	RD+	Received Data out	3	Note 4
14	VeeR	Receiver Ground	1	-
15	VccR	Receiver Power - +3.3V±5%	2	Note 5
16	VccT	Transmitter Power - +3.3 V±5%	2	Note 5
17	VeeT	Transmitter Ground	1	-
18	TD+	Transmitter Data In	3	Note 6
19	TD-	Inverse Transmitter Data In	3	Note 6
20	VeeT	Transmitter Ground	1	-

Notes:

1. TX Disable input is used to shut down the PHY. It is pulled up within the module with a 4.7 – 10K resistor.
   Low (0 – 0.8V): PHY Enabled
   Between (0.8V and 2V): Undefined
   High (2.0 – VccT): PHY Disabled
   Open : PHY Disabled
2. Mod-Def 0, 1, 2. These are the module definition pins. They should be pulled up with a 4.7KΩ-10KΩ resistor on the host board to supply less than VccT+0.3V or VccR+0.3V.
   Mod-Def 0 is grounded by the module to indicate that the module is present.
   Mod-Def 1 is clock line of two wire serial interface for optional serial ID.
   Mod-Def 2 is data line of two wire serial interface for optional serial ID.
3. LOS is an open collector output, which should be pulled up with a 4.7k~10kΩ resistor on the host board to a voltage between 2.0V and Vcc+0.3V. Logic 0 indicates normal operation; logic 1 indicates loss of signa or link down with partner l. In the low state, the output will be pulled to less than 0.8V.
4. RD-/+: These are the differential receiver outputs. They are AC coupled 100Ω differential lines which should be terminated with 100Ω differential at the user SERDES. The AC coupling is done inside the module and thus not required on the host board.

5. VccR and VccT are the receiver and transmitter power supplies. They are defined as 3.3V ±5% at the SFP connector pin. The in-rush current will typically be no more than 30mA above steady state supply current after 500ns.
6. TD-/+: These are the differential transmitter inputs. They are AC coupled differential lines with 100Ω differential termination inside the module. The AC coupling is done inside the module and is thus not required on host board.

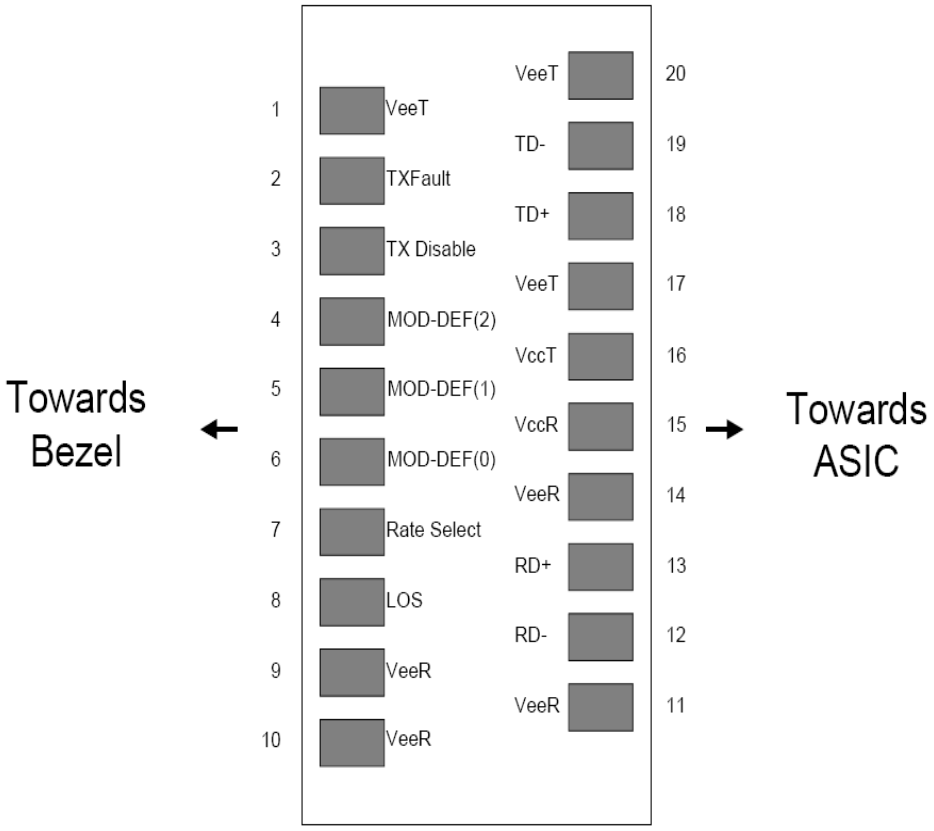

Figure 1. Diagram of Host Board Connector Block Pin Numbers and Names

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Storage Temperature	T_S	-40	85	°C
Relative Humidity	RH	5	95	%
Supply Voltage	V_{CC}	-0.5	3.6	V

Recommended Operating Conditions

Table 4. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Operating Case Temperature	T_C	-10	25	70	°C
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate	-	-	1000	-	Mb/s

Transceiver Electrical Characteristics

Table 5. Transceiver Electrical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Module Supply Current	Icc	-	-	400	mA	-
Transmitter Differential Input Voltage (TD +/-)	-	500	-	2400	mV_{P-P}	1
Receiver Differential Output Voltage (RD +/-)	-	500	-	2000	mV_{P-P}	2
Differential Input Impedance	ZTX	80	100	120	Ω	
Rise/Fall Time	Tr,Tf			250	ps	
Bit Error Ratio	BER			10^{-12}		
Low speed input: Transmitter Disable (TX_DISABLE), MOD_DEF 1, MOD_DEF 2	VIH	2.0	-	Vcc	V	3
	VIL	0	-	0.8	V	-

Notes:

1. Internally AC coupled and terminated to 100Ω differential load.
2. Internally AC coupled, but requires a 100Ω differential termination or internal to Serializer/Deserializer.
3. Mod_Def1 and Mod_Def2 must be pulled up externally with a 4.7KΩ-10KΩ resistor on the host board to $V_{CCT,R}$

EEPROM Serial ID Memory Contents

The Transceiver integrates a PHY IC which can be accessible according to 2-wire serial interface with the address of 1010110x (ACh).

Table 6. 1010110x (ACh) Serial ID Contents

Register	Description
0	Control Register
1	Status Register
2-3	N/A for SFP Module
4	Auto-Negotiation Advertisement
5	Auto-Negotiation Link Partner Ability
6	Auto-Negotiation Expansion
7	Next Page Transmit
8	Link Partner Received Next Page
9	1000BASE-T Control Register

10	1000BASE-T Status Register
11-14	N/A for SFP Module
15	Extended Status Register
16	PHY Specific Control Register
17	PHY Specific Status Register
18	Interrupt Enable Register
19	Interrupt Status Register
20	Extended PHY Specific Control Register
21	Receive Error Counter Register
22	Extended Address Register
23	Global Status Register
24-25	N/A for SFP Module
26	Extended PHY Specific Control 2 Register
27	Extended PHY Specific Status Register
28-31	N/A for SFP Module

Notes:

Register at www.marvell.com to gain access the "Alaska Ultra 88E1111 Integrated 10/100/1000 Gigabit Ethernet Transceiver" for more detail.

The transceiver also provides standard serial ID information compatible with SFP MSA, which can be accessed with address of A0h.

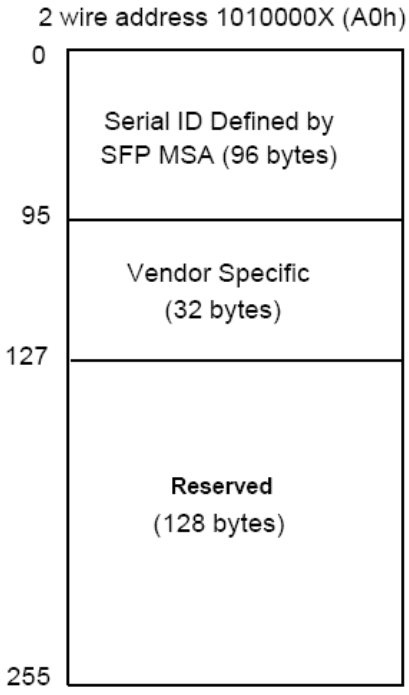

Figure 2. 1010000x (A0h) Serial ID Memory Contents

The SFP MSA defines a 256-byte memory map in EEPROM describing the transceiver's capabilities, standard

interfaces, manufacturer, and other information, which is accessible over a 2 wire serial interface at the 8-bit address 1010000X (A0h), and the clock frequency up to 100 KHz. The memory contents are shown in Table 7.

Table 7. Serial ID Memory Contents

Data Address	Name of Field	Contents(Hex)	Description
0	Identifier	03	SFP
1	Ext. Identifier	04	SFP function is defined by serial ID
2	Connector	00	
3-10	Transceiver	00 00 00 08 00 00 00 00	1000BASE-T
11	Encoding	01	8B10B
12	BR, Nominal	0D	1.25Gb/s
13	Reserved	00	
14	Length (9μm) km	00	
15	Length (9μm) 100m	00	
16	Length (50μm) 10m	00	
17	Length(62.5μm)10m	00	
18	Length (Copper)	64	100m
19	Reserved	00	
20-35	Vendor name	4C 49 4E 4B 54 45 4C 20 20 20 20 20 20 20 20 20	“LINKTEL”(ASCII)
36	Reserved	00	
37-39	Vendor OUI	00 00 00	
40-55	Vendor PN	4C 58 31 38 30 31 43 4E 4C 20 20 20 20 20 20 20	“LX1801CNL ” (ASCII)
56-59	Vendor rev	31 2E 30 20	Rev 1.0 (ASCII)
60-61	Wavelength	00 00	-
62	Reserved	00	
63	CC BASE	xx	Check sum of bytes 0 - 62
64-65	Options	00 12	
66	BR, max	00	
67	BR, min	00	
68-83	Vendor SN	xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx xx	”xxxxxxxxxx”(Customized SN, ASCII)
84-91	Vendor date code	xx xx xx xx xx xx 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes)
92	Diagnostic type	00	
93	Enhanced option	00	
94	SFF-8472	00	
95	CC_EXT	xx	Check sum for bytes 64-94
96-255		00	

Note: The “xx” byte should be filled in according to practical case. For more information, please refer to the related document of

SFF-8472 Rev 9.5.

Required Host Board Components

The MSA power supply noise rejection filter is required on the host PCB to meet data sheet performance. The MSA filter incorporates an inductor which should be rated 400mA DC and 1Ω serial resistance or better. It should not be replaced with a ferrite. The required filter is illustrated in Figure 3.

The MSA also specifies that 4.7KΩ to 10KΩ pull-up resistors for TX_FAULT, LOS, and MOD_DEF0, 1,2 are required on the host PCB. Figure is the suggested transceiver/host interface.

Figure 3 shows the recommended host board power supply circuit.

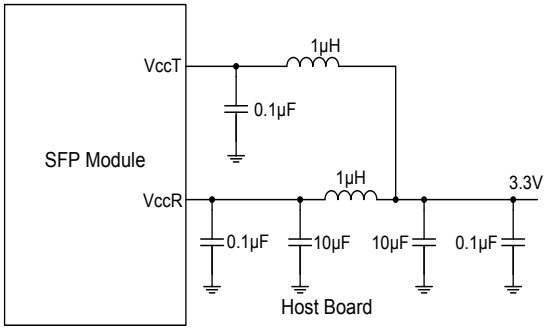

Figure 3. Recommended Host Board Power Supply Circuit

Mechanical specifications

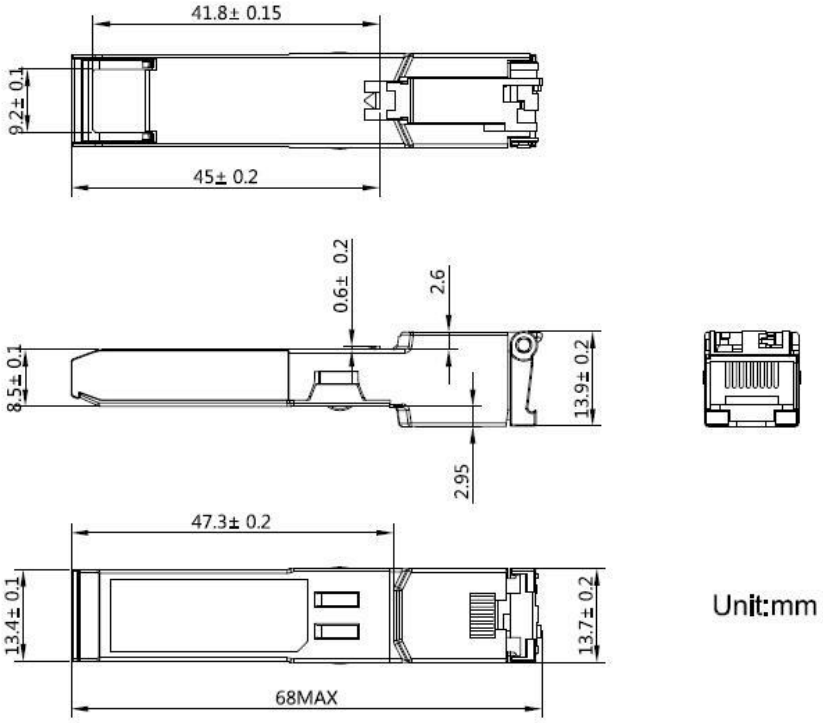

Figure 4. Outline Drawing

PCB layout recommendation

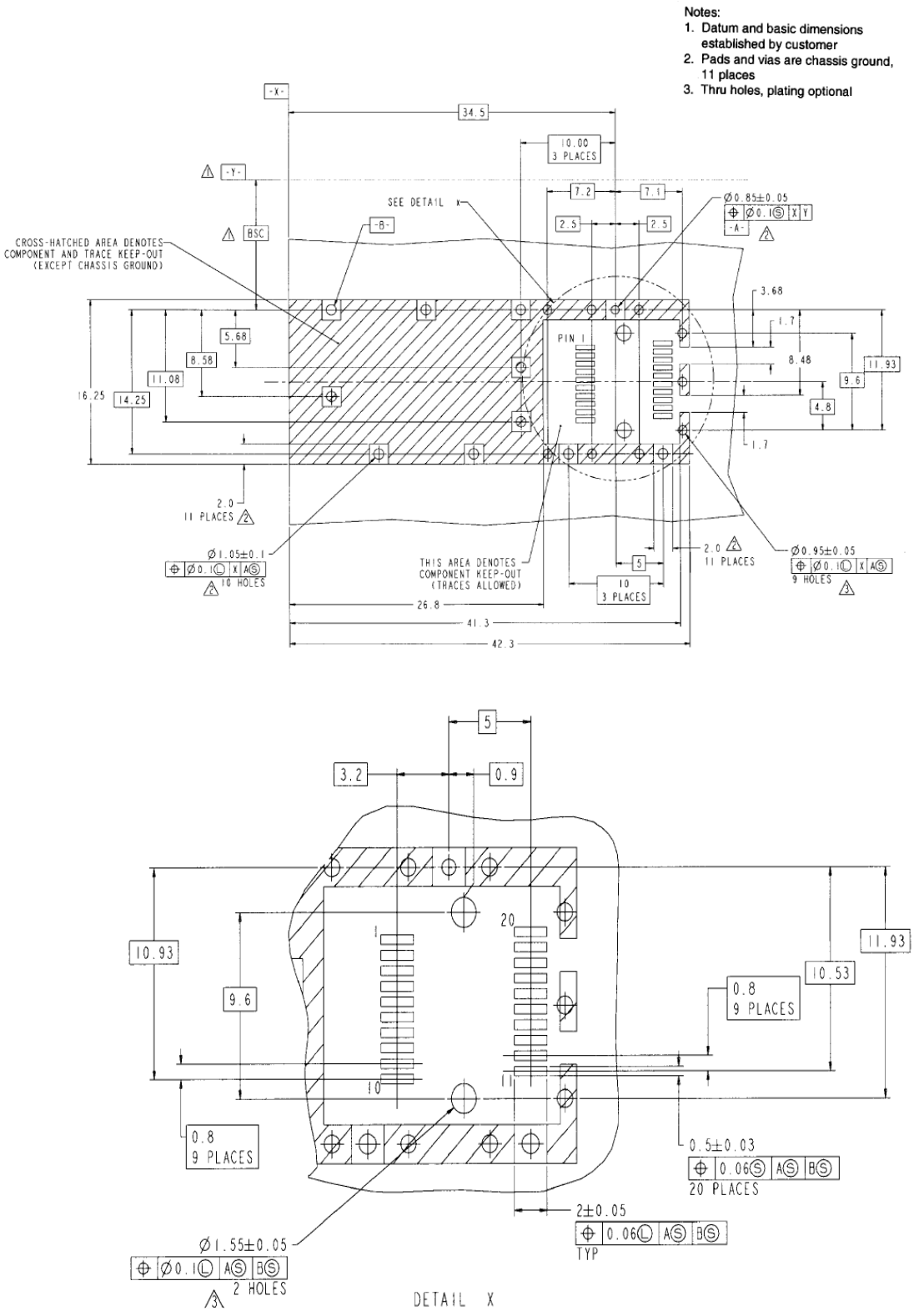

Figure 5. PCB layout recommendation

Revision History

Date	Rev	Description	Modified By
11/05/2020	V1.0	Preliminary Release	Wei Chen

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